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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,673	03/30/2004	Richard B. Irwin	TI-36795	7727

23494 7590 05/13/2005

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,673	IRWIN ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-20* is/are allowed.

6)☒ Claim(s) *1-10 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *21-30 and 32-34* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Group II, claims 1-20 and 31, in the Paper filed 03/30/05 is acknowledged.

Oath/Declaration

2. The oath/declaration filed on 06/21/2004 is acceptable.

Drawings

3. The formal drawings filed on 06/21/2004 are acceptable.

Priority

4. Applicants have made no claim for priority.

Information Disclosure Statement

5. If applicant is aware of any relevant prior art, he/she requested to cite it on form **PTO-1449** in accordance with the guidelines set forth in M.P.E.P. 609.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

A. Claims 1-3,6-8, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by TOHYAMA (5,710,447).

With regard to claims 1-3 and 6 Tohyama discloses a Schottky diode with a semiconductor substrate 1 including Si; a first metal area 14a including PtSi coupled to said semiconductor substrate 1; a barrier layer 15 including SiO_2 coupled to said first metal area 14a; and a second metal area 16 coupled to said barrier layer 15. Note figure 7B and column 7 lines 35-43 of Tohyama.

With regard to claims 7,8, and 10 Tohyama discloses a Schottky diode with a semiconductor substrate 1 including Si; a first metal area 14a including PtSi coupled to said semiconductor substrate 1; and a second metal area 16 coupled to said first metal area 14a. Note figure 7B and column 7 lines 35-43 of Tohyama.

B. Claims 1,2,4,6-8, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by WEI et al. (4,672,412).

With regard to claims 1,2,4, and 6 Wei et al. discloses a Schottky diode with a semiconductor substrate 42 including Si; a first metal area 46 including PtSi coupled to said semiconductor substrate 42; a barrier layer 50 including SiN coupled to said first metal

area 46; and a second metal area 54 coupled to said barrier layer 50. Note figure 3 and column 7 lines 5-14,29,36, and 37 of Wei et al.

With regard to claims 7,8, and 10 Wei et al. discloses a Schottky diode with a semiconductor substrate 42 including Si; a first metal area 46 including PtSi coupled to said semiconductor substrate 42; and a second metal area 54 coupled to said first metal area 46. Note figure 3 and column 7 lines 5-14,29,36, and 37 of Wei et al.

C. Claims 1,2, and 5-10 are rejected under 35 U.S.C. 102(b) as being anticipated by IRANMANESH ET AL. (5,059,555).

With regard to claims 1,2,5, and 6 Iranmanesh et al. discloses a Schottky diode with a semiconductor substrate 14 including Si; a first metal area 52 including PtSi coupled to said semiconductor substrate 14; a barrier layer 54 coupled to said first metal area 52; and a second metal area 51 including $TiSi_2$ coupled to said barrier layer 54. Note figure 1, column 4 lines 66-67, column 5 lines 51-53 and 63, and column 6 lines 1-14 of Iranmanesh et al.

With regard to claims 7-10 Iranmanesh et al. discloses a Schottky diode with a semiconductor substrate 14 including Si; a first metal area 52 including PtSi coupled to said semiconductor substrate 14; and a second metal area 51 including $TiSi_2$ coupled to said first metal area 52. Note figure 1, column 4 lines 66-67, column 5 lines 51-53 and 63, and column 6 lines 1-14 of Iranmanesh et al.

D. Claim 31 is rejected under 35 U.S.C. § 102(b) as being anticipated by LOH-STROH (4,595,942).

Lohstroh discloses an integrated circuit with a first Schottky diode 7 having a voltage drop (VD2) of 500 mV, which is more than .1% different from 350 mV, the voltage drop (V D1) of a second Schottky diode 6. Note figure 1 and column 4 lines 43-45 of Lohstroh.

The applicant's claim 31 does not distinguish over the Lohstroh reference regardless of the process used to form the integrated circuit, because only the final product is relevant, not the recited process of forming a barrier layer over said semiconductor substrate, forming a first patterned photoresist layer over said semiconductor substrate, said first patterned photoresist layer exposing different portions of a first Schottky diode and a second Schottky diode locations, forming a first metal layer over said semiconductor substrate, removing said first patterned photoresist layer; annealing said semiconductor substrate to form areas of reacted first metal and areas of un-reacted first metal, removing selected areas of said un-reacted first metal; forming a second patterned photoresist layer over said semiconductor substrate; said second patterned photoresist layer exposing different portions of said first Schottky diode and said second Schottky diode locations, f forming a second metal layer over said semiconductor substrate, removing said second patterned photoresist layer, and annealing said semiconductor substrate to form areas of reacted second metal and areas of un-reacted second metal.

Note that a "product by process" claim is directed to the product per se, no matter how actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re

Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

Allowable Subject Matter

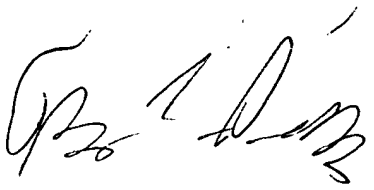
7. Claims 11-20 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as an integrated circuit comprising a semiconductor substrate; a first Schottky diode coupled to said semiconductor substrate, said first Schottky diode having a first amount of a first metal coupled to said semiconductor substrate and a second amount of a second metal coupled to said first amount of a first metal; and a second Schottky diode coupled to said semiconductor substrate, said second Schottky diode having a third amount of said first metal coupled to said semiconductor substrate and a fourth amount of said second metal coupled to said third amount of said first metal; wherein said first amount is at least .1 % more than said third amount and said second amount is at least .1 % more than said fourth amount, as recited in claims 11 and 17.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
Patent Examiner
Art Unit 2826
05/05